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HIGH VOLTAGE INTEGRATED CIRCUIT TRANSISTOR

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ABSTRACT OF THE DISCLOSURE

An integrated circuit transistor includes a substrate and an epitaxially grown semiconductor material thereon providing a three-layer transistor comprising a collector layer, an emitter layer, and a base layer therebetween. The collector layer is characterized by virtually complete depletion of majority carriers at a collector-emitter voltage less than the voltage at which collector-emitter breakdown would otherwise occur. As a result, the collector-emitter voltage may be increased without encountering normal collector-emitter breakdown, because the field intensity in the collector-base charge layer is limited.

BACKGROUND OF THE INVENTION

Typical collector-to-emitter breakdowns of integrated transistors are caused by multiplication of I_{CBO}, or leakage current, by transistor action and subsequent avalanche multiplication of this current in the collector-base space charge layer. Minority carriers traversing the collector region receive enough energy and acceleration to cause impact ionization whereby breakdown occurs. The collector-emitter voltage is, of course, normally limited by this breakdown voltage, BV_{CEO}.

SUMMARY OF THE INVENTION

According to the present invention, the collector in an integrated circuit transistor configuration is substantially depleted of majority carriers at a voltage less than the characteristic collector-emitter breakdown voltage. The collector material and doping thereof is chosen such that such depletion takes place before breakdown. As a result, the field intensity is limited in the collector-base space charge layer whereby carriers traversing the region will not receive enough energy to cause impact ionization even though the collector-emitter voltage is raised further than the characteristic collector-emitter breakdown value. As a consequence, a transistor is provided which is operative at high collector-emitter voltages, even up to the voltage at which the back-biased collector-base junction itself breaks down.

According to a preferred form of the present invention, the integrated transistor is formed directly upon a substrate providing a junction with the collector which is back-biased such as to limit the active collector region. In this manner, it is possible advantageously to reduce the effective collector region thickness in value whereby such region will be effectively depleted of charge below the normal collector-emitter breakdown voltage for the type of transistor.

It is accordingly an object of the present invention to provide an improved transistor for operation at higher collector-emitter voltages.

It is a further object of the present invention to provide an improved integrated transistor operative at voltages above what would normally be considered breakdown voltage.

It is a further object of the present invention to provide a method of operating a transistor at voltages above what would otherwise be considered breakdown values.

The subject matter which I regard as my invention is

particularly pointed out and distinctly claimed in the concluding portion of this specification. The invention, however, both as to organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings wherein like reference characters refer to like elements.

DRAWINGS

FIG. 1 is a partially broken-away cross sectional view of an integrated transistor according to the present invention, further including circuitry elements connected therewith;

FIG. 2 is a plot of D.C. common-emitter characteristics for a transistor in accordance with the present invention;

FIG. 3 is a plot of D.C. common-emitter characteristics for a similar transistor employing a buried layer, wherein the voltage and current scales are the same as in FIG. 2;

FIG. 4 is a plot of D.C. common-emitter characteristics for a different value of substrate collector bias for the FIG. 1 transistor, with the voltage and current scales being the same as in FIGS. 2 and 3; and

FIG. 5 is a circuit substantially equivalent to the circuit of the FIG. 1 transistor.

DETAILED DESCRIPTION

As illustrated in FIG. 1, an integrated circuit transistor in accordance with an embodiment of the present invention is provided with a substrate member **10** of semiconductor material which may be a part of a monolithic circuit including a plurality of other transistors (not shown). The substare member **10** may be P type silicon having a resistivity of 10 ohm-centimeters. Layer **12**, formed of N type semiconductor material and suitably having a substantially uniform resistivity of one ohm-centimeter, is provided on the upper surface of the substrate member such as by epitaxial growth with suitable impurity doping. This layer provides the collector region **14** of the transistor and is directly adjacent the P-type substrate without use of an intermediate layer, or buried layer, therebetween. Layer **12** suitably has a thickness of approximately five microns. Base and emitter layers or regions **16** and **18** are provided by diffusing appropriate doping material into the epitaxial layer in the usual manner whereby the depth of the collector-base junction **20** is approximately 1.5 microns below the top surface of the device. The sheet resistance of the base is approximately 200 ohms per square, with the emitter being approximately one micron deep and having a sheet resistance of ten ohms per square. The base is doped much more heavily than the collector. Contact **22** provides connection with the emitter region while contacts **24**, **26**, and **28** provide connection with the base, collector, and substrate regions respectively.

The base-emitter junction **30** is forward-biased by a battery **32** in series with a signal source or the like **34** disposed between contacts **22** and **24**. The collector-base junction **20** is back-biased by means of battery **36**, while the collector-substrate junction **15** is similarly back-biased with battery **38**. A load resistor **40** connects battery **36** to contact **26**. A substantially equivalent circuit for the FIG. 1 transistor is illustrated schematically in FIG. 5. Here the reference numeral **44** indicates the transistor structure of FIG. 1, and reference numeral **46** indicates the collector-substrate semiconductor junction.

The thickness t of the active collector region, i.e., the collector region beneath the emitter, and the resistivity resulting from doping thereof, are chosen such that the collector region is virtually depleted of majority carriers